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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/428,110	10/27/99	KANG Y	51876.P160

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EXAMINER	
HO,H	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 05/12/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/428,110	Kang
Examiner	**Group Art Unit**
H. Ho	2818

☒ Responsive to communication(s) filed on *10/27/99*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-13* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1, 3-5, and 7-13* is/are rejected.

☒ Claim(s) *2 and 6* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☒ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *3*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

1. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) was considered.

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

2. Claims 1-13 are presented for examination.

Drawings

3. The drawings filed on 10/27/99 are acceptable.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3, and 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Osawa US Pat. No. 5,608,667.

With regards to claims 1 and 3, Figure 2 or 5 of Osawa is directed to a ferroelectric random access memory (FeRAM) device, comprising: a plurality of memory cells (MCs) arranged in an M x J matrix (col. 1, lines 55-59), wherein M is a positive integer more than three and J is a positive integer; a number of reference cells (RMCs) connected to each column of the memory cells; and a cell selection means (1 and fig. 3) for selecting a memory cell in response to address signals from an external circuit (col. 6, lines 18-19) and selecting a reference cell corresponding to

the selected memory cell (fig. 3). See column 1, line 5 to column 2, line 10 and column 3, lines 36-58, line 65 to column 4, line 18.

With regards to claim 9, Figure 2 or 5 of Osawa discloses wherein said memory cells have one transistor (Tr1) and one ferroelectric capacitor (FC1). See column 3, lines 36-40.

With regards to claim 10, Figure 2 or 5 of Osawa discloses wherein said reference cells have one transistor (RTr1) and one ferroelectric capacitor (RFC1). See column 3, lines 47-52.

With regards to claim 11, Figure 2 or 5 of Osawa discloses wherein said memory cells are connected to first bit line (BL1). See column 3, lines 38-39.

With regards to claim 12, Figure 2 or 5 of Osawa discloses wherein said reference cells are connected to second bit line (BL2). See column 3, line 50.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 4, 5, 7, and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Osawa US Pat. No. 5,608,667 in view of Ihara US Pat. No. 5,689,468.

With regards to claim 4, Figure 2 or 5 of Osawa does not disclose wherein said memory cell selection circuit includes: a plurality of NAND gates, each NAND gate for receiving address signals from an external circuit to perform NAND logical operation; and a plurality of inverters,

each inverter for inverting an output signal of each NAND gate to generate the memory cell selection signal. However, Figure 22 of Ihara dislcoses a memory cell selection circuit includes: a plurality of NAND gates (22), each NAND gate for receiving address signals ($X_{1[0]}$-$X_{4[3]}$) from an external circuit (AND gates) to perform NAND logical operation; and a plurality of inverters (22), each inverter for inverting an output signal of each NAND gate to generate the memory cell selection signal (WL0) for the purpose of decoding the external address signals for selecting the memory cell location. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to recognize that Osawa could have the memory cell selection circuit constructed by a plurality of NAND gates and a plurality of inverter gates to generate the memory cell selection signal as taught by Ihara in order to decode the external address signals for selecting one of the memory locations in the ferroelectric random access memory (FeRAM) device.

With regards to claim 5, Figure 2 or 5 of Osawa and Ihara do not disclose wherein said reference cell selection circuit includes: a plurality of NANDgates, each NAND gate for receiving address signals from an external circuit to perform NAND logical operation; and a plurality of inverters, each inverter for inverting an output signal of each NAND gate to generate the reference cell selection signal. Figure 22 of Ihara only dislcoses a memory cell selection circuit includes: a plurality of NAND gates (21), each NAND gate (21a) for receiving address signals ($X_{1[0]}$-$X_{4[3]}$) from an external circuit (AND gates) to perform NAND logical operation; and a plurality of inverters (22), each inverter (21b) for inverting an output signal of each NAND gate

to generate the reference cell selection signal (RD01) for the purpose to decode the external address signals for selecting the memory cell. However, one of ordinary skill would have found it obvious to use the same circuit concept to construct the reference cell selection circuit for generating the reference cell selection signal as well. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to recognize that Osawa could have the memory cell selection circuit constructed by a plurality of NAND gates and a plurality of inverter gates to generate the reference cell selection signal as taught by Ihara in order to decode the external address signals for selecting one of the reference locations in the ferroelectric random access memory (FeRAM) device.

With regards to claim 7, Osawa and Ihara do not disclose wherein each NAND gate of said memory cell selection circuit has eight input terminals. However, Figure 22 of Ihara disclose each NAND gate (in 22) of said memory cell selection circuit has four input terminals connected to the four row address lines from each of four row address lines will have 256 word lines to be specified (col. 36, lines 43-58). It would have been an obvious matter of design choice to have each NAND gate having four or eight input terminals, since such a modification would have involved a mere change in a number of input terminals of NAND gate depended on the size of the ferroelectric random access memory (FeRAM) device. A change in input terminals of NAND gate is generally recognized as being within the level of ordinary skill in the art.

With regards to claim 8, Osawa and Ihara do not disclose wherein each NAND gate of said reference cell selection circuit has three input terminals. Figure 22 of Ihara disclose each

NAND gate (in 22) of said memory cell selection circuit has four input terminals using for generating the memory cell selection signal. However, one skill in the art could use the same circuit concept to construct the reference cell selection circuit for generating the reference cell selection signal as well. It would have been an obvious matter of design choice to have each NAND gate has four or three input terminals, since such a modification would have involved a mere change in a number of input terminals of NAND gate depended on the size of the reference memory cells. A change in input terminals of NAND gate is generally recognized as being within the level of ordinary skill in the art.

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Osawa US Pat. No. 5,608,667 in view of Evans, Jr. US Pat No. 5,963,466.

Osawa does not disclose wherein said memory cells and said reference cells shares a cell plate, wherein the cell plate is positioned between the first bit line and the second bit line.

However, Osawa, starting column 4, lines 15-18 and lines 38-41, discloses that a cell plate of the memory cells and the reference cells is controlled by a signal PL and a signal RPL. As illustrated in Figure 3, the signals PL and RPL have the same timing pulse. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the memory cells and the reference cells sharing the cell plate by connecting the cell plate PL of the memory cell and the cell plate RPL of the reference memory cell together as the claimed invention, since the signals PL and RPL which control the cell plates PL and RPL have the same timing pulse as shown in Osawa's Figure 3 and would perform the same functions to control the

common cell plate of the memory cells and the reference cells for reading or writing. For example of sharing the common cell plate, Figure 1 of Evans, Jr. discloses the memory cells (20) and the reference cells (connection to 13D) sharing a cell plate (16 and its title). It would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Osawa which utilizes the memory cells and the reference cells sharing the cell plate as taught by Evans Jr., because Evans, Jr. suggests that in order to avoid the additional masks and deposition steps needed to construct the ferroelectric capacitors and make the connections to the plate lines increase the cost and lower the yield of devices (col. 2, lines 16-20). The higher yield and the reduction of in cost in the ferroelectric random access memory (FeRAM) device would have been motivated an artisan at the time the invention was made to follow Evans, Jr. teachings in Osawa ferroelectric random access memory (FeRAM) device.

Evans, Jr. and Osawa do not disclose wherein the cell plate is positioned between the first bit line and the second bit line. It would have been an obvious matter of design choice to each plate line is parallel to each word line as Osawa teachings (col. 2, lines 14 and 15) and Evans, Jr. teachings (col. 7, lines 9-21), or as the claimed invention, since applicant has not disclosed that the cell plate is positioned between the first bit line and the second bit line solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the cell plate is positioned between the first bit line and the second bit line.

9. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Jung (5,959,922) dislcoses a ferroelectric random access memory device with reference cell array blocks.

Allowable Subject matter

10. Claims 2 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

Claims 2 and 6 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Osawa (5,608,667), Evans, Jr. (5,963,466), Ihara (5,689,468), and Jung (5,959,922), taken individually or in combination, do not teach the claimed invention having wherein the number of memory cells of each column is $M = 2^N$ and the number of reference cells is N in claim 2; or wherein the number of the memory cells is 2^8 and the number of the reference cells is eight in claim 6.

12. When responding to the office action, Applicants' are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

13. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (703) 308-4839. The examiner can normally be reached on Mon. - Thur. from 7:00 A.M. to 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached on (703) 308-4910. The fax phone number for this Group is (703) 308-7722. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

HHH

H. Ho

April 20, 2000

Hoaivanho

Hoai V. Ho

Patent Examiner

Group 2800